SIE 370
Embedded Computer Systems
Spring 2019

Class Hours: Mondays and Wednesdays at 1:00 - 2:30 PM
Lab Hours: Fridays at 1:00 – 4:00 PM
Classroom: EB 128
Laboratory: EB 128
Instructor: Samuel Peffers, EB 122, (928) 317-7067, samuelpeffers@email.arizona.edu
Office Hours: M,W, F 8:30 – 10:00 AM, or by appointment

Course Description: Boolean algebra, combinational and sequential logic circuits, finite state machines, simple computer architecture, assembly language programming, and real-time computer control. The computer is used as an example of systems engineering design; it is analyzed as a system, not as a collection of components. There is a lab associated with this course.

Prerequisites: ENGR102 and ENGR 211M or ECE 207, or articulated equivalents.

Course objectives:
1. Understand number systems, Boolean algebra, Karnaugh maps, and digital logic design program so that you can design, build and test digital circuits.
2. Know how to devise a state machine to describe the actions of a microcontroller based system.
3. Understand how to translate a software implementation of a system into a hardware implementation or vice-versa.
4. Construct actual microprocessor systems using integrated circuit devices, clocks, and other electrical components.
5. Know how to analyze a problem that can be solved using a digital logic system and successfully design that system.

Textbooks:

Lee, E. & Seshia, S. (2015). *Introduction to Embedded Systems - A Cyber-Physical Systems Approach, 2nd Ed.* Berkley, CA: LeeSeshia.org

ISBN: 978-1-312-42740-2

A copy of this book and other materials are all available on D2L; D2L is the primary means of distributing class material.

Absence and Class Participation Policy:
Participating in course and attending lectures and other course events are vital to the learning process. As such, attendance is required at all lectures and discussion section meetings. Students who miss class due to illness or emergency are required to bring documentation from their healthcare provider or other relevant, professional third parties. Failure to submit third-party documentation will result in unexcused absences.

The UA's policy concerning Class Attendance, Participation, and Administrative Drops is available at: http://catalog.arizona.edu/2015-16/policies/classatten.htm

The UA policy regarding absences for any sincerely held religious belief, observance or practice will be accommodated where reasonable, http://policy.arizona.edu/human-resources/religious-accommodation-policy.

Absences pre-approved by the UA Dean of Students (or Dean Designee) will be honored. See: http://uhap.web.arizona.edu/policy/appointed-personnel/7.04.02

Classroom Behavior Policy:
To foster a positive learning environment, students and instructors have a shared responsibility. We want a safe, welcoming and inclusive environment where all of us feel comfortable with each other and where we can challenge ourselves to succeed. To that end, our focus is on the tasks at hand and not on extraneous activities (i.e. texting, chatting, reading a newspaper, making phone calls, web surfing, etc). Students are asked to refrain from disruptive conversations with people sitting around them during lecture. Students observed engaging in disruptive activity will be asked to cease this behavior. Those who continue to disrupt the class will be asked to leave lecture or discussion and may be reported to the Dean of Students.

Threatening Behavior Policy:
The UA Threatening Behavior by Students Policy prohibits threats of physical harm to any member of the University community, including to one's self. See: http://policy.arizona.edu/education-and-student-affairs/threatening-behavior-students.

Accessibility and Accommodations:
Our goal in this classroom is that learning experiences be as accessible as possible. If you anticipate or experience physical or academic barriers based on disability, please let me know immediately so that we can discuss options. You are also welcome to contact Disability Resources (520-621-3268) to establish reasonable accommodations. For additional information on Disability Resources and reasonable accommodations, please visit http://drc.arizona.edu/.
If you have reasonable accommodations, please plan to meet with me by appointment or during office hours to discuss accommodations and how my course requirements and activities may impact your ability to fully participate. Please be aware that the accessible table and chairs in this room should remain available for students who find that standard classroom seating is not usable.

Code of Academic Integrity:
Students are encouraged to share intellectual views and discuss freely the principles and applications of course materials. However, graded work/exercises must be the product of independent effort unless otherwise instructed. Students are expected to adhere to the UA Code of Academic Integrity as described in the UA General Catalog. See: http://deanofstudents.arizona.edu/academic-integrity/students/academic-integrity.

UA Nondiscrimination and Anti-Harassment Policy:
The University is committed to creating and maintaining an environment free of discrimination, http://policy.arizona.edu/human-resources/nondiscrimination-and-anti-harassment-policy

Subject to Change Statement:
Information contained in the course syllabus, other than the grade and absence policy, may be subject to change with advance notice, as deemed appropriate by the instructor.

Assessment and Deliverables:

Product	Percentage of Course Grade	
Mid-term Exam		15%
Final Exam		20%
Quizzes / Homework (lowest five scores)		ea. 2%
Lab Products & Reports (ten scores)		ea. 1%
Term Project Milestones (lowest four scores out of five graded milestones other than DAR)		
Proposal		
	Written	3%
	Oral	2%
Requirements Validation Review (RVR)		
	Written	3%
	Oral	2%
Systems Architecture Review (SAR)		
	Written	3%
	Oral	2%
Critical Design Review (CDR)		
	Written	3%
	Oral	2%
Test Readiness Review (TRR)		
	Written	3%
	Oral	2%
Design Acceptance Review (DAR)		
	Written	10%
	Product	10%
	Oral	5%

Grading Scale:

A: 90 – 100
B: 80 – 89
C: 70 – 79
D: 60 – 69
F: 0 – 59

Course Schedule:

Date	Activity / Topic	Reading
Jan 9, 2019	Embedded systems and Arduino fundamentals	Read: *L&S*, Chpt. 1; Review: *APN*
Jan 11, 2019	**Lab 1**: Course intro, laboratory safety, procedures, simple circuits	See D2L
Jan 14, 2019	The design process	Read: *ISEHB* 5-21, 25-32; Review: *NSEHB* 282-283
Jan 16, 2019	Digital input to digital output	Read: *L&S* 261-272; Review: *APN* 23-24
Jan 18, 2019	**Lab 2**: Digital input to digital output	See D2L
Jan 23, 2019	Analog input to analog out put	Read: *L&S* 177-194; Review: *APN* 25-26
Jan 25, 2019	**Lab 3**: Analog input to analog out put	See D2L
Jan 28, 2019	**Project proposal presentations**	See D2L
Jan 30, 2019	Analog input to digital output	Review: *APN* 24-25
Feb 1, 2019	**Lab 4**: Analog input to digital output	See D2L
Feb 4, 2019	Technical Processes 4.1, 4.2, & 4.3	Read: *ISEHB* 47-64
Feb 6, 2019	Digital input to analog output	Read: https://www.arduino.cc/en/Reference/Tone
Feb 8, 2019	**Lab 5**: Digital input to analog output	See D2L
Feb 11, 2019	**Requirements Validation Review (RVR)**	See D2L
Feb 13, 2019	Rotary motor control	Read: *L&S* 201-205; https://www.arduino.cc/en/Tutorial/TransistorMotorControl
Feb 15, 2019	**Lab 6**: Rotary motor control	See D2L
Feb 18, 2019	Technical Processes 4.4; state machines	Read: *ISEHB* 64-70; *L&S* 49-64 Review: *L&S* Chpts 4, 5
Feb 20, 2019	Servo motor control	Read: https://www.arduino.cc/en/Reference/Servo, Include information at links
Feb 22, 2019	**Lab 7**: Servo motor control	See D2L
Feb 25, 2019	**System Architecture Review (SAR)**	See D2L
Feb 27, 2019	Stepper motor control	Read: https://www.arduino.cc/en/Reference/Stepper, Include information at links
Mar 1, 2019	**Lab 8**: Stepper motor control	See D2L
Mar 11, 2019	Technical Process 4.5	Read: *ISEHB* 70-74

Mar 13, 2019	LCD displays	Read: https://www.arduino.cc/en/Reference/LiquidCrystal, Include information at links
Mar 15, 2019	**Lab 9**: Visual display control	See D2L
Mar 18, 2019	**Mid-term Exam**	See D2L
Mar 20, 2019	Multifunctional control	Read: *L&S* 293-318
Mar 22, 2019	**Lab 10**: Multifunctional control	See D2L
Mar 25, 2019	**Critical Design Review (CDR)**	See D2L
Mar 27, 2019	Technical Processes 4.9 and 4.11	Read: *ISEHB* 83-87, 89-95
Mar 29, 2019	In lab project build / test time	IAW project plan
Apr 1, 2019	Boolean algebra	See D2L
Apr 3, 2019	Karnaugh maps	See D2L
Apr 5, 2019	In lab project build / test time	IAW project plan
Apr 8, 2019	**Test Readiness Review (TRR)**	See D2L
Apr 10, 2019	Logical architecture and logic circuits	Read: *L&S* 360-369
Apr 12, 2019	In lab project build / test time	IAW project plan
Apr 15, 2019	Circuit design	See D2L
Apr 17, 2019	Systems Modeling	Read: *L&S* 386-396, 511-517
Apr 19, 2019	In lab project build / test time	IAW project plan
Apr 22, 2019	Design Acceptance Review discussion / preparation	See D2L
Apr 24, 2019	**Final Exam**	See D2L
Apr 26, 2019	In lab project build / test time	IAW project plan
May 1, 2019	**Design Acceptance Review (DAR)**	See D2L